

Patent infringement discovery in integrated circuits: a new approach

I. Introduction

While reverse engineering approaches to Intellectual Property (IP) protection have progressed little over the last 25 years, a little more could be said for the use of automated tools. In a typical patent infringement case involving integrated circuits, definitive proof of patent infringement may lie in the physical fabricated semiconductor Integrated Circuits (IC)s. Equally damaging proof of patent infringement or non-infringement, as the case may be, may lie in the database files that describe the circuitry, assuming they are provided or ordered for evidence by the court. In many of these cases, careful review of graphical schematics may reveal the circuits in question by visually comparing symbolic circuitry to the claims language in the patent.

The traditional method for creating a schematic from an actual integrated circuit is done by a combination of chemical stripping processes and manual optical inspection. One may draw circuit schematics by hand by observing with a microscope the tiny connections within an integrated circuit. The drawn schematic becomes the highest level document from which to make comparisons against the claims language. This can be a time consuming process, prone to error, and must follow very specific steps at very specific locations within an integrated circuit to avoid costly delays in the investigation. Additionally one must interpret the patent language before beginning the reverse engineering process, to allow the investigators to focus their resources on specific circuit areas within the chip and to resolve potential problems early.

A much simpler approach will serve when schematics of the devices are available. In such cases one may compare schematics directly to the patent language without costly manual search procedures. While this approach may seem robust and complete, there are still other techniques which may prove advantageous when the chip netlist or chip database is provided.

With a full chip netlist or graphical database (GDS) in evidence, new techniques can be applied to discovery and reverse engineering. These techniques mirror a class of circuit verification tools, long established in the IC design industry known as Layout Versus Schematic (LVS). LVS tools can determine whether a schematic netlist or synthesized netlist matches perfectly with the drawn geometries of the chip, thus are vital for circuit verification. However, they cannot find a sub-circuit within a larger circuit; thus also they cannot tell how many occurrences of a smaller circuit exist within the larger one.

A new tool, CSIP (Chip Search for Intellectual Property), finds these sub-circuits. It not only provides a thorough search of the netlist or provided GDS file, it will also find all instances of such circuits regardless of their physical location in the chip database. It does this in an environment which is sufficiently versatile to allow on-the-fly adjustments to the circuit under pursuit, and can provide graphic illustrations which highlight identified circuit locations.

II. Comparison

Technique	Speed	Accuracy	Patent Language Interpretation
Optical Inspection, reverse engineering of circuits	Slow	Suspect	Patent language should be interpreted before reverse engineering begins.
Schematic Inspection	Nominal	Nominal	Patent language should be interpreted along with investigation of schematics.
Automated netlist or GDS searching	Fast	Exact	Patent language may be interpreted later allowing greater freedom in searching the domain of potential infringers.

Table I

Table 1 compares three patent infringement discovery techniques, made possible by availability of three types of material. The traditional technique involves reverse engineering acquired product material; the other techniques are possible when schematics documents or database materials are available.

III. Examples

Figure 1 shows a machine routed logic block. These are dense connections of logic gates used for general purpose logic functions within a chip. These blocks can hold hundreds of thousands of logic gates and are virtually impossible to trace by hand. Figure 2, for example, shows a schematic of a small sub-circuit to be used in a search. A schematic tool creates the netlist; the search tool processes both this netlist and a large place and route block, to produce a list of potential circuit matches. These matches take graphic form as the black dots in Figure 3; zooming into one of those dots shows a collection of silicon devices which precisely map to the input circuit, Figure 4.

Note, from Figure 2, that the schematic contains devices and interconnects that should be found in the place and route database. However, it may be unclear that the I/O points of the circuit may be able to connect to an infinite number of other circuits or devices. Labeling the circuit nodes with a + in front of the label accommodates a large fan-out; in this way we allow larger and more general circuits to be built.

The technique succeeds with large databases, and is fast. It relies on the degrees of the circuits initially and the topology secondarily, to quickly scan the circuit space. This means that it first pre-processes the netlist to sort nets by their degree of connectivity to devices. It then searches these degrees with the target circuit as the search criteria. When degrees match, it parses the target search tree, which allows it to quickly eliminate many initial matches that do not meet the criteria of the target circuit topology. It makes final matches only when it finds an exact topology.

Further filtering of initial matches may then be necessary due to duplicate circuit matching, which may occur when symmetry is present in the topology. Additional filtering may be useful when the patent language clearly eliminates circuits with shorted or grounded inputs, or which have any number of other conditions.

Finally, when applying these techniques to the GDS as the initial input, a graphical output may identify the locations of the circuits in question as demonstrated in

Figure 4 for the example schematic of Figure 2. The above technique has been used on GDS files greater than 1GByte in size successfully.

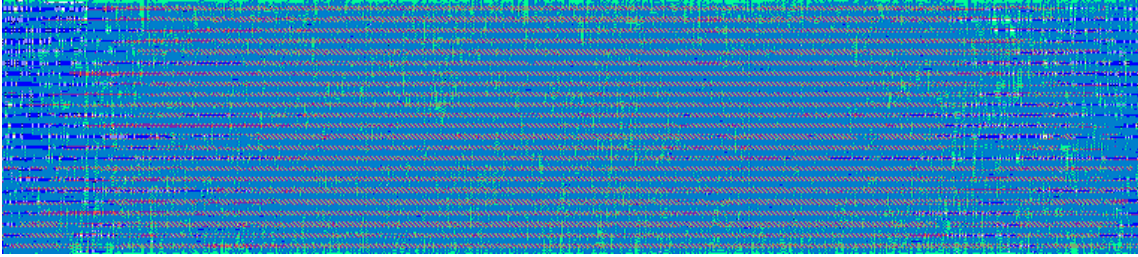


Figure 1. Logic block containing over 26000 logic cells.

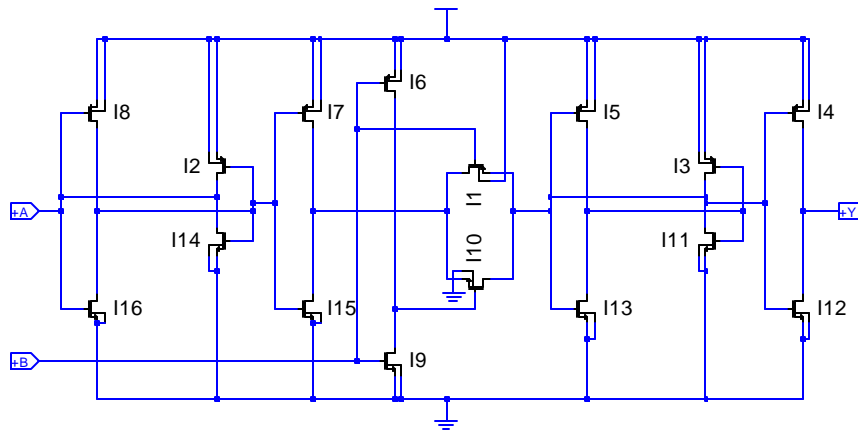


Figure 2. Simple sub-circuit schematic

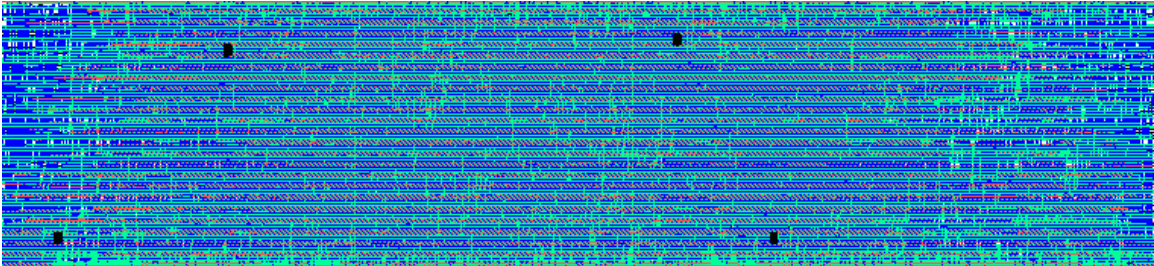


Figure 3. Identified circuits in large place and route block

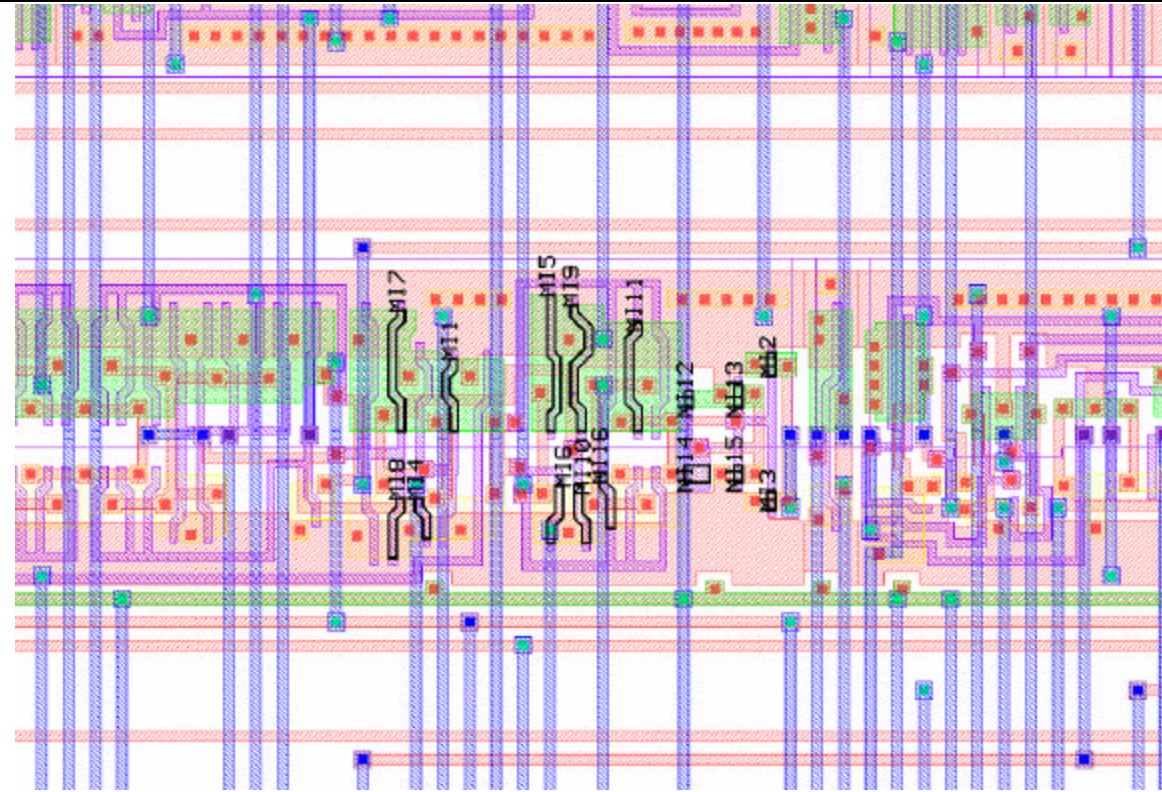


Figure 4. Zoom showing outlined transistor in found circuit

IV. Conclusion

The CSIP tool can reduce the cost of circuit discovery in potential patent infringement cases and gives the user both greater flexibility and faster response while patent language interpretation is still in flux. The examples shown are representative of actual cases, which involved successful processing of GDS files of size greater than 1 GByte. And although not demonstrated in this paper, the same technique can be used on RTL or gate level netlists to perform the same function.